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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,971	01/29/2004	Jeffrey H. Dreibelbis	BUR920030154US1	1970

29154 7590 01/30/2007

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/707,971	DREIBELBIS ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/15/04 & 1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed January 29, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-6 & 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okitaka US Pat no. 6,343,366 B1.

As per claim 1:

Okitaka substantially teaches a hybrid built-in self test (BIST) architecture (Figure 5) for embedded memory arrays (Figure 5 # 51, column 9, lines 25-28) that segments BIST functionality into remote lower-speed executable instructions (Figure 4 # 1) and local higher-speed executable instructions (Figure 5 # 1), the architecture comprising: a standalone BIST logic controller (Figure 4 # 1) operating at a lower frequency and being adapted to communicate with a plurality of embedded memory arrays using a BIST instruction set (columns 9-10, lines 63-9); and a block of higher-speed test logic (Figure 5 # 9) incorporated into each embedded memory array under test (Figure 5 # 51) and being adapted to locally process BIST instructions received from said standalone BIST logic controller at a higher frequency than said lower frequency (column 9, lines 35-40).

Okitaka does not teach the location of the frequency multiplier to be in the block of higher speed test logic. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the PLL in the Memory Cell Array after the BIST, since it has been held that rearranging parts of an invention involves only routine skill in the art. In *re Japikse, 86 USPQ 70.* Further it should be noted that the BIST in the third embodiment of Okitaka is operational at a low frequency, hence the above claim can also be rejected under Okitaka by combining the third and fourth embodiment of Okitaka (column 1, lines 2-5), since one of ordinary skill in the art would have recognized that including the PLL after the BIST controller would have been obvious because doing so would have allowed for the BIST to work at the same lower frequency of the external device (column 9, lines 33-37), hence improving the efficiency of the testing procedure.

As per claim 2:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 1, wherein said higher-speed test logic includes a multiplier (Figure 5 # 9, column 9. lines 50-53) for increasing the frequency of said BIST instructions from said lower frequency to said higher frequency.

As per claim 3:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 1 wherein said standalone BIST logic controller enables a plurality of higher-speed test logic structures in a plurality of embedded memory arrays (column 10, lines 3-13).

As per claim 4:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 1, wherein said standalone logic controller enables testing of different types of embedded memories (column 9, lines 25-29).

As per claim 5:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 1, further comprising a lower-speed control bus operating at said lower frequency and (Figure 5, the signal between # 9 & # 1, column 9, lines 55-58) connecting said standalone BIST logic controller to said higher-speed test logic (Figure 5, the signal between # 1 & # 2, column 9, lines 64-67).

As per claim 6:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 1, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM) (column 13, lines 24-26), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets (column 10, lines 3-15).

As per claim 8:

Okitaka substantially teaches a built-in self test (BIST) architecture (Figure 5) for use with memory arrays (Figure 5 # 51) embedded in functional circuitry within an integrated circuit, said BIST architecture comprising: a plurality of embedded blocks of test logic incorporated into embedded memory arrays (Figure 5 # 51, column 9, lines 25-30); a remote BIST logic controller (Figure 5 # 1), separate from said embedded blocks of test logic (Figure 5 # 51); and a bus connecting said remote BIST logic controller to said embedded blocks of test logic (Figure 5 signal between #1, #2, & # 3,

column 9, lines 64-67, the BIST is connected indirectly but the BIST is essentially transmitting the signal which ultimately initiates the self-test mode), wherein said remote BIST logic controller performs functions that are common to all of said embedded blocks of test logic (column 9-10, lines 59-16), and wherein said remote BIST logic controller and said bus operate at a lower frequency than said embedded blocks of test logic (the same arguments as pertaining to the frequency changes and location of parts of claim 1).

As per claim 9:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 8, wherein said higher-speed test logic includes a multiplier (Figure 5 # 9, column 9. lines 50-53) for increasing the frequency of said BIST instructions from said lower frequency to said higher frequency.

As per claim 10:

Okitaka substantially teaches the BIST architecture in claim 8, wherein each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array (column 2, lines 25-30). (The same arguments as pertaining to the frequency changes and location of parts of claim 1).

As per claim 11:

Okitaka substantially teaches the BIST architecture in claim 8, wherein each of said embedded blocks of test logic includes: a clock multiplier (Figure 5 # 9); redundancy allocation logic (Figure 5 # 8, column 10, lines 50-59); data address control generation logic (column 4, lines 54-60); and decoding logic adapted to decode macro

instruction sets received from said remote BIST logic controller into multiple individual micro instructions (Figure 5 # 2, column 10, lines 5-10).

Again the same arguments pertaining to the location of parts such as clock multiplier, redundancy logic, and data address logic, holds. The essential concept and functioning of the invention is the same but the location of the parts is changed, which requires routine skill in the art.

As per claims 12:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 8, wherein said standalone logic controller enables testing of different types of embedded memories (column 9, lines 25-29).

As per claim 13:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 8, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM) (column 13, lines 24-26), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets (column 10, lines 3-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7, 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okitaka US Pat no. 6,343,366 B1, in view of Hirabayashi US PG Pub no. 20020170003 A1 and further in view of Tran US Pat no. 5961634 A.

As per claim 7:

Okitaka substantially teaches the hybrid BIST architecture in claim 1 wherein said standalone BIST logic controller comprises logic adapted to general BIST operation controls (column 9, lines 63-66) and diagnostic outputs (Figure 5 # 8).

Okitaka does not teach the use of counters and it does not exactly teach branch prediction techniques.

However, Hirabayashi in an analogous art teaches a semiconductor circuit which employs the use of a counter (Figure 4 # 142). It would have been obvious to one of ordinary skill in the are to include a counter within the hybrid BIST architecture of Okitaka, since one of ordinary skill in the art would have recognized that including a counter would have enabled Okitaka's invention to keep track of the number of the number of faulty memory cells that have been replaced by the redundant memory cells (column 10, lines 55-59). Doing so would allow for an accurate analysis of the performance of the invention. Further it should be noted that the use of a counter during testing procedures is a commonly employed procedure and there are an excess amount of inventions that employ the use of a counter during testing procedures involving a BIST.

Tran in an analogous art teaches a microprocessor which employs the techniques of branch prediction (Figure 1 # 14). It would have been obvious to one of ordinary skill in the art to include branch prediction techniques within the hybrid BIST architecture of Okitaka, since one of ordinary skill in the art would have recognized that including branch prediction techniques within the teaching of Okitaka would have contributed in an increase in the performance of branched sections of code. Further branch predictions execute code in advance to allow for the appropriate output to be on hand when required. This function is already being performed in Okitaka's invention,

where the test pattern generator outputs the expected value data (column 10, lines 5-12).

Okitaka teaches the claimed invention except for in the location of the frequency multiplier is before the BIST as opposed to in the block of higher speed test logic. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the PLL in the Memory Cell Array after the BIST, since it has been held that rearranging parts of an invention involves only routine skill in the art. In *re Japikse, 86 USPQ 70.* Further it should be noted that the BIST in the third embodiment of Okitaka is operational at a low frequency, hence the above claim can also be rejected under Okitaka by combining the third and fourth embodiment of Okitaka (column 1, lines 2-5), since one of ordinary skill in the art would have recognized that including the PLL after the BIST controller would have been obvious because doing so would have allowed for the BIST to work at the same lower frequency of the external device (column 9, lines 33-37), hence improving the efficiency of the testing procedure.

As per claim 14:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 8, 1 wherein said standalone BIST logic controller comprises logic adapted to general BIST operation controls (column 9, lines 63-66) and diagnostic outputs (Figure 5 # 8).

Okitaka does not teach the use of counters and it does not exactly teach branch prediction techniques.

However, Hirabayashi in an analogous art teaches a semiconductor circuit which employs the use of a counter (Figure 4 # 142). It would have been obvious to one of ordinary skill in the are to include a counter within the hybrid BIST architecture of Okitaka, since one of ordinary skill in the art would have recognized that including a counter would have enabled Okitaka's invention to keep track of the number of the number of faulty memory cells that have been replaced by the redundant memory cells (column 10, lines 55-59). Doing so would allow for an accurate analysis of the performance of the invention. Further it should be noted that the use of a counter during testing procedures is a commonly employed procedure and there are an excess amount of inventions that employ the use of a counter during testing procedures involving a BIST.

As per claim 15:

Okitaka substantially teaches a built-in self test (BIST) architecture (Figure 5) for use with memory arrays (Figure 5 # 51) embedded in functional circuitry within an integrated circuit, said BIST architecture comprising: a plurality of embedded blocks of test logic incorporated into embedded memory arrays (Figure 5 # 51, column 9, lines 25-30); a remote BIST logic controller (Figure 5 # 1), separate from said embedded blocks of test logic (Figure 5 # 51); and a bus connecting said remote BIST logic controller to said embedded blocks of test logic (Figure 5 signal between #1, #2, & # 3, column 9, lines 64-67, the BIST is connected indirectly but the BIST is essentially transmitting the signal which ultimately initiates the self-test mode), wherein said remote BIST logic controller and said bus operate at a lower frequency than said

embedded blocks of test logic (the same arguments as pertaining to the frequency changes and location of parts of claim 1), wherein said remote BIST logic controller performs functions that are common to all of said embedded blocks of test logic (column 9-10, lines 59-16) including providing branch prediction, program counter management, utility counting (The same argument pertains from claim 7), and general BIST operation controls (column 9, lines 63-66) and diagnostic outputs (Figure 5 # 8).

As per claim 16:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 15, wherein said higher-speed test logic includes a multiplier (Figure 5 # 9; column 9. lines 50-53) for increasing the frequency of said BIST instructions from said lower frequency to said higher frequency.

As per claim 17:

Okitaka substantially teaches the BIST architecture in claim 15, wherein each of said embedded blocks of test logic includes unique logic blocks that are unique to a corresponding embedded memory array (column 2, lines 25-30). (The same arguments as pertaining to the frequency changes and location of parts of claim 1).

As per claim 18:

Okitaka substantially teaches the BIST architecture in claim 15, wherein each of said embedded blocks of test logic includes: a clock multiplier (Figure 5 # 9); redundancy allocation logic (Figure 5 # 8, column 10, lines 50-59); data address control generation logic (column 4, lines 54-60); and decoding logic adapted to decode macro

instruction sets received from said remote BIST logic controller into multiple individual micro instructions (Figure 5 # 2, column 10, lines 5-10).

Again the same arguments pertaining to the location of parts such as clock multiplier, redundancy logic, and data address logic, holds. The essential concept and functioning of the invention is the same but the location of the parts is changed, which requires routine skill in the art.

As per claim 19:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 15, wherein said standalone logic controller enables testing of different types of embedded memories (column 9, lines 25-29).

As per claim 20:

Okitaka teaches the hybrid BIST architecture as shown in the rejection of claim 15, wherein said standalone BIST logic controller comprises at least one of a read only memory (ROM) (column 13, lines 24-26), a scannable read only memory (SROM), and other type of memory adapted to store macro instruction sets (column 10, lines 3-15).

As per claim 21:

Okitaka substantially teaches the hybrid BIST architecture in claim 15 wherein said standalone BIST logic controller comprises logic adapted to general BIST operation controls (column 9, lines 63-66) and diagnostic outputs (Figure 5 # 8).

Okitaka does not teach the use of counters and it does not exactly teach branch prediction techniques.

However, Hirabayashi in an analogous art teaches a semiconductor circuit which employs the use of a counter (Figure 4 # 142). It would have been obvious to one of ordinary skill in the are to include a counter within the hybrid BIST architecture of Okitaka, since one of ordinary skill in the art would have recognized that including a counter would have enabled Okitaka's invention to keep track of the number of the number of faulty memory cells that have been replaced by the redundant memory cells (column 10, lines 55-59). Doing so would allow for an accurate analysis of the performance of the invention. Further it should be noted that the use of a counter during testing procedures is a commonly employed procedure and there are an excess amount of inventions that employ the use of a counter during testing procedures involving a BIST.

Tran in an analogous art teaches a microprocessor which employs the techniques of branch prediction (Figure 1 # 14). It would have been obvious to one of ordinary skill in the art to include branch prediction techniques within the hybrid BIST architecture of Okitaka, since one of ordinary skill in the art would have recognized that including branch prediction techniques within the teaching of Okitaka would have contributed in an increase in the performance of branched sections of code. Further branch predictions execute code in advance to allow for the appropriate output to be on hand when required. This function is already being performed in Okitaka's invention, where the test pattern generator outputs the expected value data (column 10, lines 5-12).

As per claim 22-35:

These claims are directed to a method of the system of Claims 1-21. Okitaka, Hirabayashi, and Tran either alone or in combination as stated above, teach the system as set forth in Claims 1-21. Therefore, Okitaka, Hirabayashi, and Tran also teach, either alone or in combination as stated above, the method as set forth in claims 22-35.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US PG-Pub no.20030034791 A1, US PG-Pub no. 20050120270 A1, US PG-Pub no. 20040085082 A1, and US Pat no. 6779144 B2 mention the same BIST procedure which includes the modifications of frequency during the testing procedure are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS Cynthia Britt

Saqib Siddiqui
Art Unit 2138
02/15/2006